

9-5-00

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

"Express Mail" Mailing Label
Number: EF07384083/US
Date of Deposit: 8/31/2000

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to this Commissioner of Patents and Trademarks Washington, D.C. 20231
Ferdinand M. Romano
Printed name of person mailing paper or fee
Ferdinand M. Romano
Signature of person mailing paper or fee

PATENT APPLICATION

Allen Yen
Frank Yauchee Hui
Yifeng Winston Yan

CASE 3-6-16

TITLE Stacked Structure For Parallel Capacitors And Method Of Fabrication

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR § 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification
10 Informal Sheets of drawing(s)

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	10 - 20 =	0	x \$18 =	\$0
Independent Claims	2 - 3 =	0	x \$78 =	\$0
Multiple Dependent Claims, if applicable			+ \$260 =	\$0
Basic Fee				\$690
			TOTAL FEE	\$690

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of \$690, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

The Assistant Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Please address all correspondence to **Docket Administrator (Room 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P.O. Box 636, Murray Hill, New Jersey 07974-0636**. However, telephone calls should be made to me at 407-371-3250.

Respectfully,

Ferdinand M. Romano
Ferdinand M Romano
Reg. No. 32752
Attorney for Applicant(s)

ORIGINAL FORM

Date: 8/31/2000

Lucent Technologies Inc.
600 Mountain Avenue (Room 3C-512)
P.O. Box 636
Murray Hill, New Jersey 07974-0636

08/31/00
jc511 U.S. PTO

jc511 U.S. PTO
09/653295
08/31/00

Stacked Structure for Parallel Capacitors and Method of Fabrication

Field of the Invention

5 The present invention relates to semiconductor devices and, more specifically, to devices having capacitor structures formed in metallization levels over a semiconductor layer.

Background of the Invention

10 As the level of semiconductor process integration has progressed, advances in the technology have been largely focused on reducing feature sizes and layout geometry of active devices as well as increasing the density of metallization. However, in many instances, reductions in the area requirements for passive devices have not kept pace with reduced feature sizes of active devices and metallization. For example, the layout area required for resistors is largely determined by the sheet resistance. The physical size of a
15 capacitor network is limited by several factors, including the required area of the capacitor plates as well as the thickness of the intervening dielectric. That is, as dielectric thickness decreases the capacitance increases such that the capacitor becomes less area consuming. Generally, reduction in layout area for resistor and capacitor structures has been largely considered a function of material selection. There is a need to provide
20 additional methods and designs so that further reductions in area requirements of passive structures will not depend solely on development of new materials. In particular, further reduction in area requirements for capacitors will enable further in the level of integration for both digital and analog circuitry. Prior efforts to increase capacitance without increasing area consumed over a semiconductor region where effected by forming
25 multiple capacitors on separate metal levels and connecting these in parallel.

In the past , in order to provide increased capacitance to meet circuit requirements, capacitors formed on separate metal levels have been wired in parallel circuitry. Another means of achieving high capacitance has been reduction in the thickness of the dielectric layer between the capacitor plates.

5 **Summary of the Invention**

According to illustrated embodiments of the invention a semiconductor device includes first and second levels of interconnect conductor for connection to a semiconductor layer. A stack of alternating conductive and insulative layers is formed in vertical alignment with respect to an underlying plane. The stack, formed between the
10 first and second levels of conductor, includes a first conductive layer, a first insulator layer formed over the first conductive layer, a second conductive layer formed over the first insulative layer, a second insulator layer formed over the second conductive layer, and a third conductive layer formed over the second insulative layer. The first and third conductive layers are commonly connected.

15 According to an associated method for making a semiconductor device with a capacitor structure one embodiment includes forming a first conductive runner on a first insulative layer and forming a second conductive runner above the first conductive runner. A stack of alternating conductor and dielectric layers is formed between the first conductive runner and the second conductive runner and an opening is etched in an
20 upper-most of the conductive layers. The opening is extended through an adjoining dielectric layer to a first underlying conductor layer.

Brief Description Of The Drawings

Numerous advantages of the invention will be apparent when the following detailed description of the invention in conjunction with the accompanying drawings in which:

5 Figure 1 illustrates in partial cross-sectional view one embodiment of the invention;

 Figures 2-7 illustrate fabrication steps leading to formation of the Figure 1 embodiment;

 Figure 8 illustrates an alternate preferred embodiment of the invention;

10 Figure 9 illustrates another alternate embodiment of the invention; and

 Figure 10 illustrates still another alternate embodiment of the invention.

 Like numbers refer to like elements throughout the drawings while it should be noted that various features illustrated in the figures are not drawn to scale with one another.

15 **Detailed Description**

 With reference to the view of Figure 1, the invention is described with respect to formation and connection of an exemplary capacitor structure formed in three levels of interconnect metallization. A portion of an integrated circuit structure 10 is shown in partial cross section to provide details of the invention in a metallization structure. The
20 metallization structure is formed over a semiconductor layer (not illustrated) which typically will have a plurality of transistors in the surface thereof. In this exemplary embodiment, several upper levels of metal interconnect, such as Al or Cu runners, are formed over the semiconductor layer according to a dual Damascene fabrication process.

Specifically, a portion of the integrated circuit structure 10 is shown in Figure 1 to include three sequentially formed levels of metallization 20, 30 and 40. One or more additional levels of metallization may be formed below level 20 and one or more additional levels of metallization may be formed above level 40. Generally, the metal runners in each level are formed along a plane such as illustrated by line 42 along level 20. For purposes of illustrating the invention a capacitor structure 50 is electrically connected to conductors in the illustrated levels of metallization. The capacitor structure 50 includes alternating layers of conductor and insulator formed in vertical alignment with respect to an underlying plane such as plane 42 or the plane of the surface on which the structure is formed. The structure 50 is wired to provide two capacitors in parallel. Three conductor layers 52, 54, and 56 are isolated from one another by two intervening dielectric layers. One dielectric layer 58 is formed between conductors 52 and 54 and the other dielectric layer 60 is formed between conductor layers 54 and 56.

In the illustrated structure 50 the conductor layer 54 is a capacitor plate common to a first capacitor formed with layers 52 and 58 and a second capacitor formed with layers 56 and 60. A via portion 64 of metallization level 40 contacts the conductor layer 54 to provide a common terminal for both capacitors. Another via portion 66 of metallization level 40 makes connection with the conductor layer 56 to provide a second terminal for the capacitor formed by layers 54, 56 and 60. A conductor runner portion 68 of metallization level 30 provides connection to the conductor plate layer 52 to provide a second connection the capacitor formed by layers 52, 54 and 58.

A via portion 72 in metallization level 30 connects the conductive runner portion 68 to a conductive runner 74 in metallization level 20. The conductor runner 74 is

connected through another via portion 72 to conductive runner portion 76 of level 30. A via portion 78 of level 40 connects the conductive runner portion 76 to the conductive runner 82 of level 40 to effect contact through the via portion 66 to the capacitor conductor 56. A via portion 94 (associated with an overlying level of metallization) provides connection of the plates 52 and 56 to other circuitry not illustrated. Alternately, this connection could be made to a lower level of metallization through the conductive runner 74 of level 20. A via portion 96 (also associated with an overlying level of metallization) provides connection of the common plate 54 through a conductive runner 98 of level 40 to other circuitry not illustrated.

10 The Damascene structure within which the exemplary capacitor 50 is formed is well known and is only briefly described. Generally, the exemplary embodiments, each level of metallization is formed with an initial deposit of a dielectric layer such as the layer 70 of Figure 2 . The level 20 of metallization is completed prior to formation of the capacitor structure 50. The layer 70 of dielectric material will typically be multi-layered, formed with an etch stop such as silicon nitride and planarized by chemical mechanical polishing (CMP). Desired configurations of the Cu conductor lines are patterned and etched in the dielectric material to form trench-like openings therein. Commonly, conductive barrier material (not illustrated) such as Ta, TaN or TiN is deposited along the surfaces of the etched opening to prevent migration of copper which is subsequently deposited in the openings. The barrier metal may be formed with chemical vapor deposition (CVD) or physical vapor deposition (PVD).

The Cu deposition is initiated with deposit of a seed layer on the barrier material, followed by electro-plating of Cu (e.g., from Copper sulfate) to fill the openings. For

dual Damascene structures such as the illustrated level 20, both the via portion (providing connection between different levels of metallization) and the conductor portion (providing conductor runners within a level of metallization) are formed in sequential pattern and etch steps, followed by deposit of the barrier layer material, a seed layer and then an electro-deposition of the Cu to completely fill the via portions and the conductor member portions of the openings. After Cu deposition, an anneal may be provided to stabilize the micro structure. The structure is polished to remove excess copper and barrier metal from the surface of the dielectric layer 70. This sequence is repeated for each level of metallization until the final copper layer of interconnection is passivated and the structure is prepared for packaging and assembly.

Once the dual Damascene level 20 is completed the layers of conductor 52, 54, and 56 and intervening dielectric layers 58 and 60 are deposited. See Figure 3. The conductor layers 52, 54, 56 may be formed of sputtered Ta or TaN or TiN. These layers may be deposited by physical vapor deposition (PVD) or chemical vapor deposition (CVD). Preferably, the conductor layer 52 will comprise a Ti/TiN or Ta/TaN stack to provide a diffusion barrier and assure suitable adhesion of the conductor layer 52 with the underlying dielectric layer 70. By way of example, a Ti/TiN stack having approximately 20 nm of Ti and approximately 40 nm of TiN, may be deposited by a sequential sputter at 400C, followed by an anneal. The layers 54 and 56 may also be deposited by sputter techniques with the identified materials. However, a wide variety of other conductive materials are suitable. The dielectric layers 58 and 60 may be silicon oxides deposited by CVD. The oxide may be formed from silane. Alternately, the dielectric layers 58 and 60

may be formed of TaO_5 . Other insulator materials may be chosen based on desired dielectric constants and requirements regarding minimum current leakage.

With reference to Figures 4 and 5, the upper most conductor layer 56 is patterned and etched to remove a portion thereof and begin formation of an opening 88 to provide electrical connection to the underlying layer 54. After the opening 88 is formed through the layer 56 for connection to the layer 54 all of the layers 52, 54, 56, 58 and 60 are patterned and etched in vertical alignment to fully define the capacitor structure 50. That is, the etch defines vertically aligned layers with respect to an underlying plane such as the plane 42 or the plane along the surface of the dielectric layer 70 on which the structure 50 is formed. See next Figure 6, which illustrates a 60 nm barrier layer 80 of silicon nitride deposited on the exposed portions of layers 52, 54, 56, 58 and 60 as well as the dielectric layer 70 and exposed regions of Cu in the metallization level 20. See Figure 5.

With reference to Figure 6 another dielectric layer 90 is formed over the structure 10 by a conformal deposition such as high density plasma (HDP) deposition of silicon oxide. The dielectric layer 90 is planarized by CMP, or by metal topographic reduction (MTR), wherein deposit of photoresist over low regions is followed by a standard etch. The planarized structure, ready for formation of the metallization level 40, is illustrated in Figure 7.

The via portions 64 and 66 and conductor members 82 and 98 of metallization level 40 are then formed in the dielectric layer 90 as illustrated in Figure 1.

The capacitor structure 50 may also be connected in the circuit structure 10 with two levels of interconnect conductors as illustrated in Figure 8. A lower conductor level

30 includes a runner portion 124 effecting connection between lower plate 52 and a via portion 92 of level 40. Other connections are as described with regard to Figure 1.

In other embodiments of the invention stacks of three, four and more capacitors can be fabricated in parallel connection with such stacks formed between two levels of conductor. See Figure 9 which illustrates a stack comprising five conductor layers 122 sequentially deposited with intervening dielectric layers 124 positioned between pairs of layers 120 to provide capacitor dielectrics. Connections to individual layers 122 are made through via portions 126 and conductive runners 120, 123 and 124 to configure four capacitors connected in parallel.

10 The principles shown in dual Damascene embodiments may also be readily applied to Al interconnect in a conventional subtractive metal etch process. See Figure 10 which illustrates the capacitor structure 250 including three sequentially formed metal layers 252, 254, and 256 with two intervening dielectric layers 262 positioned between pairs (252, 254) and (254, 256) of layers to provide capacitor dielectric. The structure 15 250 is connected to configure two parallel capacitors. The lowest level 252 metal layer may be a runner in a level 270 of Al interconnect comprising Al - Cu alloy with an underlayer of Ti/TiN providing adhesion and a barrier against diffusion. The level 270 is formed over a dielectric layer 272. The layers 254 and 256 may be deposited TiN. A second level 280 of Al interconnect is formed above the structure 250 in a dielectric layer 20 284. Contacts 286 extend through an interlevel dielectric layer 288 to configure the parallel capacitors in connection with two runners 290 and 292 in level 280. Alternately, all of the layers of the capacitor structure 250 may be formed in vertical alignment, with

the contact between runner 290 and layer 252 made through a connection to a metal runner below the level 270 (not illustrated).

An architecture has been described which is useful for high density formation of capacitor structures in integrated circuits. Application of the disclosed design and

5 fabrication methods may be made to a variety of digital and analog circuit applications, including memory circuits which utilize capacitors and analog circuitry which demands large values of capacitance. The specific metal and insulator materials disclosed are exemplary, as are the specific interconnect patterns shown for configuring parallel capacitors. However, the principles disclosed herein provide a basis for practicing the

10 invention in a variety of ways on a variety of circuit structures, including structures formed with other materials, such as compound structures. Numerous variations will be apparent to those skilled in the art. Thus, other constructions, although not expressly described herein do not depart from the scope of the invention which is only limited by the claims which follow.

We claim:

1. A semiconductor device comprising:

at least first and second levels of interconnect conductor for connection to a semiconductor layer; and

a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane and formed between the first and second levels of conductor, including

a first conductive layer,

a first insulator layer formed over the first conductive layer,

a second conductive layer formed over the first insulative layer ,

a second insulator layer formed over the second conductive layer, and

a third conductive layer formed over the second insulative layer,

with the first and third conductive layers commonly connected.
2. The device of claim 1 wherein the first and third conductive layers are commonly connected through the first and second levels of interconnect conductor.
3. The device of claim 1 further including a third level of interconnect conductor with the first and second conductor layers commonly connected through the first, second and third levels of interconnect conductor.
4. The device of claim 1 wherein the conductors connecting the first and third conductive layers include via portions and trench portions of a Damascene structure.
5. The device of claim 1 wherein the stack of alternating conductive and insulative layers includes one or more pairs of additional conductive and insulative layers formed

over the third conductive layer providing an uppermost conductive layer commonly connected with the first and third conductive layers.

6. The device of claim 5 wherein the stack comprises 5 conductive layers configured to provide 4 capacitors connected in parallel.

7. A method for making a semiconductor device with a capacitor structure, comprising:

providing a first insulative layer;

forming a first conductive runner on the first insulative layer;

forming a second conductive runner above the first conductive runner;

forming a stack of alternating conductor and dielectric layers between the first conductive runner and the second conductive runner; and

etching an opening in an upper most of the conductive layers and extending the opening through an adjoining dielectric layer to a first underlying conductor layer.

8. The method of claim 7 further including the step of connecting the upper most of the conductive layers with a conductor layer below the first underlying conductor layer.

9. The method of claim 8 wherein the stack is formed by depositing first, second and third conductor layers and the step of connecting the uppermost conductor layer includes connecting the first conductor layer to the third conductor layer.

10. The method of claim 8 wherein the stack is formed by sequentially depositing first, second, third, fourth and fifth conductor layers separated from one another by intervening dielectric layers and the step of connecting the upper most layer includes connecting the first, third and fifth layers in common.



Lucent Technologies
Bell Labs Innovations

Bell Labs Innovations

[illegible]

Microelectronics Group

2. Cu3 CMP

3. Metals and MOM oxide deposition

10/1

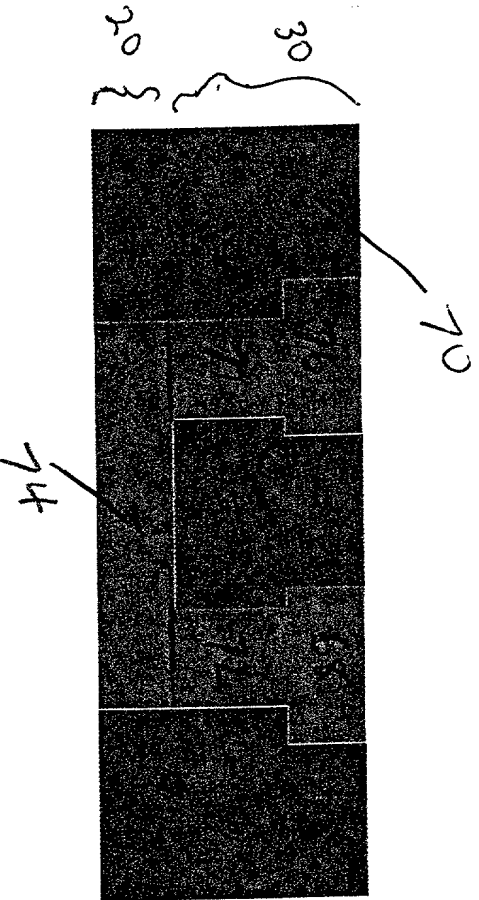


FIGURE 2

10/1

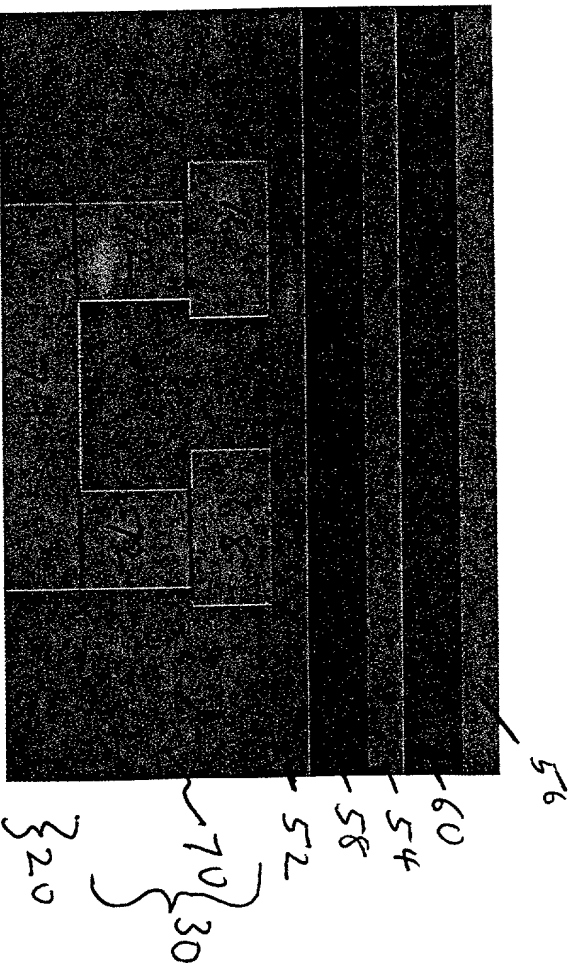


FIGURE 3

Fig. 2&3

Lucent Technologies Inc..

Lucent Technologies
Bell Labs Innovations



4. Notch etch for contact to metal B

74

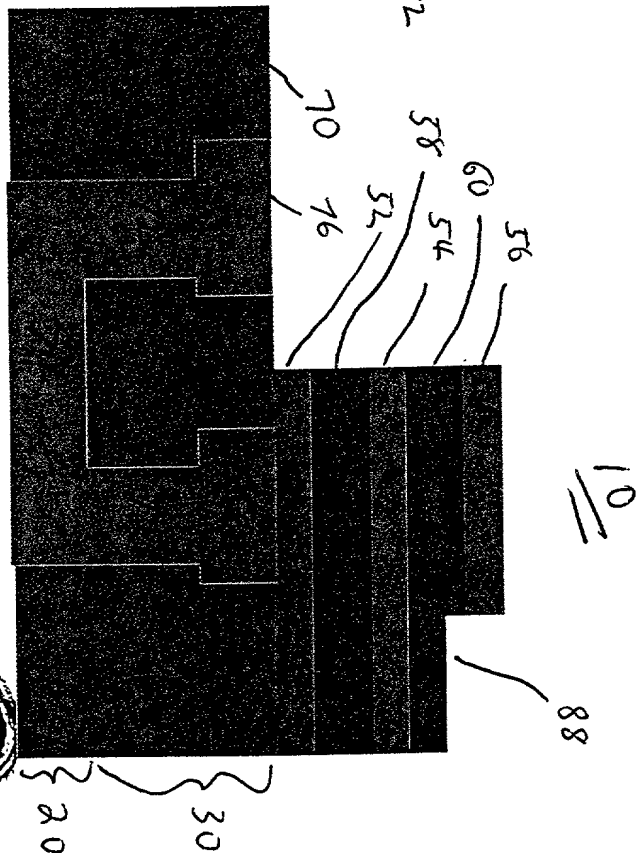


FIGURE 5

Fig. 4&5

Lucent Technologies Inc..

Microelectronics Group

8. Another version of doublemonom

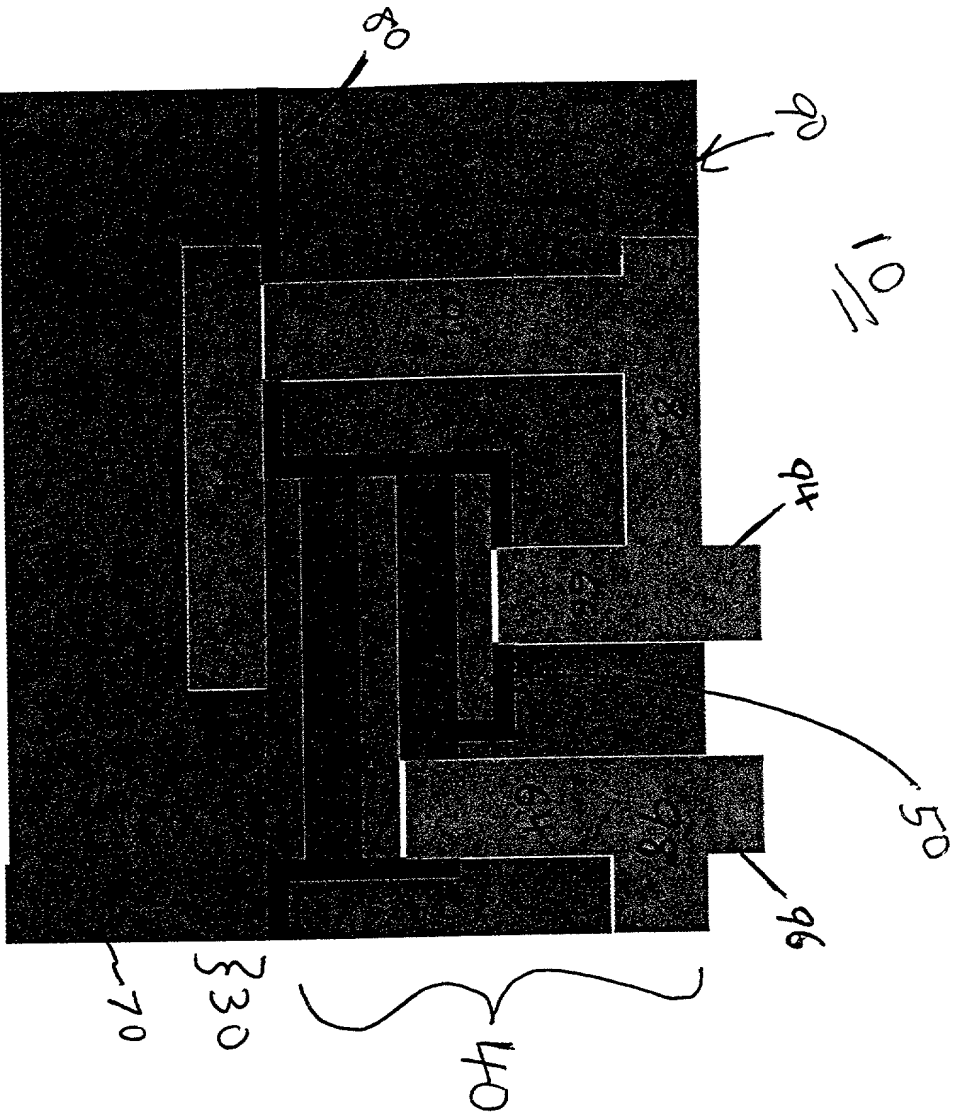
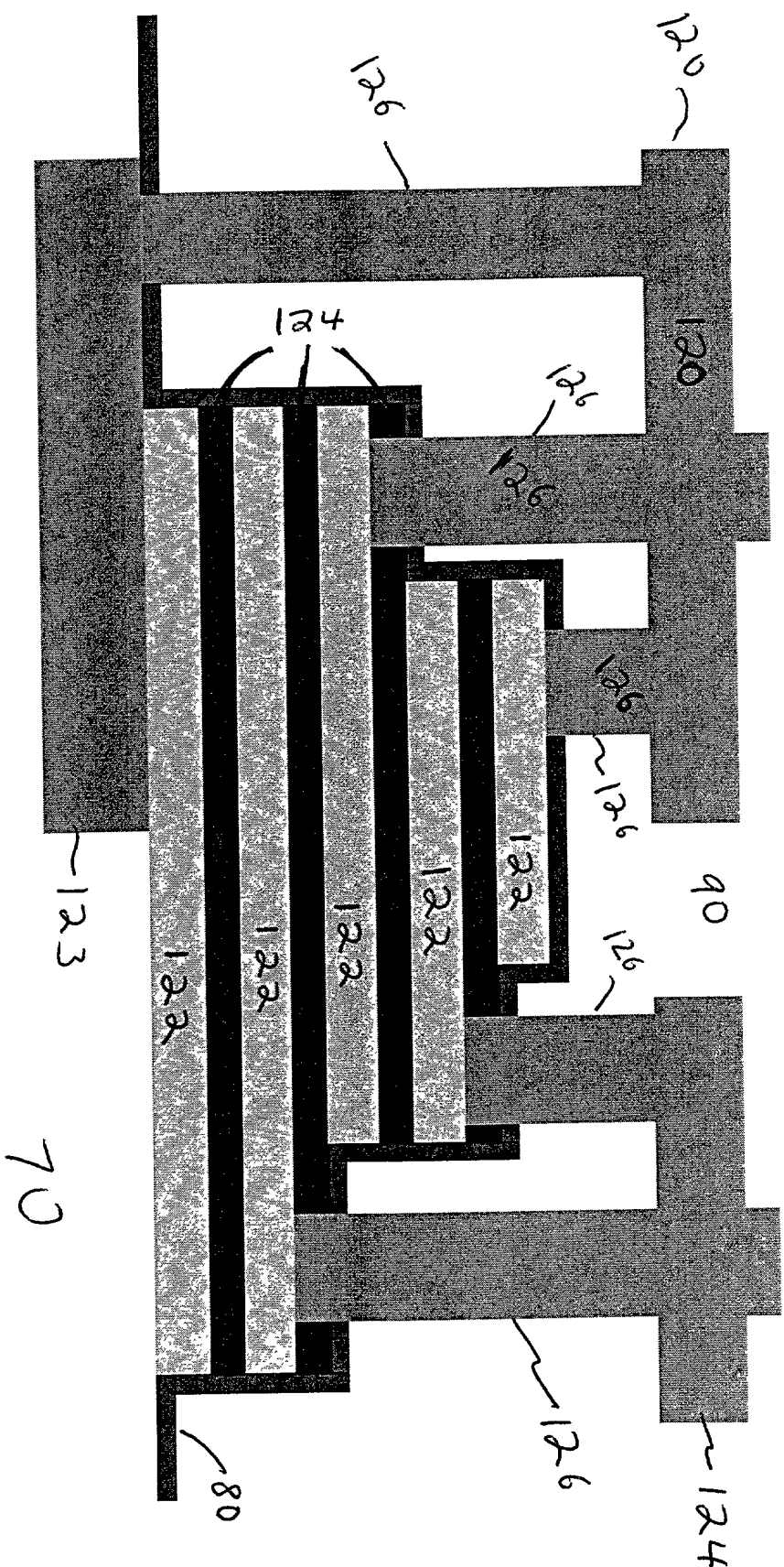


Figure 8

Lucent Technologies Inc..

Lucent Technologies
Bell Labs Innovations





F16URE9

Fig. 9

Lucent Technologies Inc..

Lucent Technologies
Bell Labs Innovations



Figure 10
250



Lucent Technologies Inc..